A Single-Phase Grid-Connected Photovoltaic Inverter Based on a Three-Switch Three-Port Flyback With Series Power Decoupling Circuit

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***Abstract*—In this paper, a novel single-stage three-port inverter that connects photovoltaic (PV) panel to a single-phase power grid is introduced. In a single-phase grid-connected PV panel, the input power is constant during the line-frequency period, while the output power oscillates at double-line frequency. A series active power decoupling circuit utilizing thin-film capacitors is incorporated to a conventional flyback inverter to handle input and output power differences. Therefore, popularly low-reliable electrolytic capacitors are replaced with small long-lifetime thin film. The proposed inverter can extract the maximum power from PV, deliver a low total harmonic distortion sinusoidal current to the output, and decouple the input and output powers. The proposed power decoupling circuit shares the inverter main switch. Thus, these functions are achieved using just three switches and a simple control scheme which is applicable for both charging and discharging states. Operation principle and control strategy are discussed in detail. Experimental results based on a 100-W prototype inverter verify feasibility and functionality of the proposed inverter.**

***Index Terms*—AC module inverter, grid connected, photovoltaic (PV), power decoupling circuit, single phase, three switch.**

Nomenclature

C_1	Decoupling capacitor.
C_{PV}	Filter capacitor in parallel with the PV panel.
C_{S_1}	Snubber capacitor.
C_f	Output filter capacitance.
L_f	Output filter inductance.
L_m	Transformer magnetizing inductance.
L_l	Transformer leakage inductance.
n_{12}	Transformer turn ratio n_1/n_2.
n_{13}	Transformer turn ratio n_1/n_3.
n_{23}	Transformer turn ratio n_2/n_3.
i_{in}	Input current of the inverter.
i_{Lm}	Current flowing through magnetizing inductance.
i_{Lp}	Current flowing through transformer primary winding.
i_{C_1}	Current flowing through decoupling capacitor.
i_{PV}	Current flowing through PV panel.
i_O	Inverter current before filtering.
i_{out}	Inverter current delivering to the grid.
V_{out}	Grid voltage.
V_{PV}	Voltage of PV panel.
P_{PV}	PV output power.
P_{PD}	Power that decoupling circuit delivers.
P_{out}	Power that inverter delivers to the grid.
ω	Angular frequency of the grid voltage.
V_m	Amplitude of the grid voltage.
I_m	Amplitude of the injected current.
T_{line}	Period of the grid voltage.
$I_{\mathrm{peak}_{11}}$	Maximum current of transformer input winding during mode 1.
$I_{\mathrm{peak}_{12}}$	Maximum current of transformer input winding during mode 4.
$I_{\mathrm{peak}_{21}}$	Maximum current of transformer output winding during mode 3.
$I_{\mathrm{peak}_{22}}$	Minimum current of transformer output winding during mode 3.
f	Switching frequency.
T	Switching period.
$d_1 - d_3$	Duty cycles of switches $S_1 - S_3$.
d'	Subtraction of d_2 (d_3) and d_1; $d' = d_2 - d_1$.
V_{SS}	Voltage of switch S_1 in mode 3.
V_{dd}	Voltage of switch S_1 in mode 4.
V_{pp}	Steady-state voltage of switch S_1 at mode 5.
$\omega_0\,(\omega_0')$	Angular resonance frequency in mode 2 (mode 5).
$Z_1\,(Z_1')$	Characteristic impedance in mode 2 (mode 5).

Manuscript received April 18, 2016; revised July 10, 2016 and August 29, 2016; accepted September 11, 2016. Date of publication October 27, 2016; date of current version February 9, 2017.

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Digital Object Identifier 10.1109/TIE.2016.2620100

I. Introduction

CURRENTLY, inverters for photovoltaic (PV) systems are categorized into three types: centralized inverter, string inverter, and ac module [1]. Recently, the ac module has attracted the attention of both researchers and industry due to its numerous advantages, such as: 1) improved energy harvest, 2) improved system efficiency, 3) low installation costs, 4) plug-n-play operation, and 5) enhanced flexibility and modularity. With these advantages, the ac module has become the trend for future PV system development [2].

In order to provide maximum power point tracking (MPPT), improve the inverter performance, and inject a sinusoidal current to the grid, several power decoupling circuits have been proposed, which can be classified as: 1) passive power decoupling circuits with passive components and 2) active decoupling circuits with semiconductor switches [3]–[8].

In the passive power decoupling circuits, a large storing device, typically electrolytic capacitor, is used to handle the input and output power differences. When a PV with 100 W and 60 V is connected to a 50-Hz grid via an ac module, decoupling capacitor must be larger than 2650 μF in order to keep the voltage ripple below 2 V. Although electrolytic capacitors have high energy density, their reliabilities are low [9], [10]. Electrolytic capacitors' lifetime are relatively short compared with the PV panels', typically 1000–7000 h at the operating temperature of 105 $^{\circ}$C. Moreover, according to the Arrhenius equation, the electrolytic capacitors' lifespan will be halved as a result of each 10° increment in temperature [11]–[13].

Recently, some active power decoupling methods have been proposed to overcome this problem. In the output-side power decoupling, the decoupling capacitor is usually embedded in the inverter stage and bidirectional switches are required. In [14]–[16], a three-leg current-source inverter has been implemented, where the third leg is responsible for power decoupling. A voltage-source version of this inverter has been proposed by Shimizu *et al.* [17] and Tsuno *et al.* [18]. A differential buck converter is designed in [19] and [20] in which filter capacitors are connected to output terminals and negative dc bus in order to store pulsating energy. Serban [21] has introduced an H-bridge inverter wherein two decoupling capacitors are placed between the midpoint and one end of each inverter leg.

In the input-side power decoupling, the capacitors are placed at the PV side. They are classified as series and parallel methods. A parallel power decoupling using active filter concept is introduced in [8], [22], and [23]. Shimizu *et al.* [24] have introduced a flyback-type double-stage ac-link inverter. In [12], a parallel power decoupling using a six-switch inverter has been introduced that can recycle the energy of a leakage inductance. A modified version of this power decoupling is proposed in [25] with five switches. A combination of boost and flyback transformer has been suggested in [26] based on a capacitive idling technique. These microinverters process power in two stages: energy capture of PV using MPPT and power delivery using a power decoupling technique. Shinjo *et al.* [27] have proposed a push–pull type forward converter with power decoupling capability.

In [28]–[33], Cai *et al.* have proposed three-port topologies in which one port implements MPPT, the second port is responsible for power decoupling, and the third one transfers power to the output. They feature few component counts and more compact structure which is one of the best candidates for power decoupling in a single-stage inverter. In [28], a four-switch three-interface dc/dc/ac converter has been proposed which can be connected to dc source, decoupling the capacitor and the ac port, but no isolation is provided between the input and output ports. Chen and Liao [29] have introduced a nine-switch three-port flyback inverter, where an H-bridge inverter controls power flow of the decoupling capacitor. Hu *et al.* [30] have offered another form of a three-port ac module that uses four switches. It has two different operating modes according to the input and output power differences. A flyback-based inverter utilizing four switches is proposed in [31] and [32], which is able to recover the leakage inductance energy of transformer without extra elements. Although it can achieve power decoupling, its control algorithm is complicated and it is vulnerable to the circuit parameter variation. Hirao *et al.* [33] have proposed a three-port flyback microinverter with both sequential and time-shared magnetizing modulation. Since the energy of a leakage inductance cannot be recycled, the overall efficiency of this circuit is not above 73%. Moreover, there are voltage spikes on the switches.

Instead of using paralleled circuit configurations, as discussed earlier, a series power decoupling technique has been suggested in [3] and [34], which is based on a current-source inverter with an active buffer.

Wang *et al.* [35] have proposed a series compensation approach where a controlled voltage source, consisting of an H-bridge inverter and a power decoupling capacitor, is inserted between the dc-link capacitor and the load. Although the dc-link voltage at the output is smooth, the low-frequency ripple voltage before the controlled voltage source still exists. This may affect the MPPT function and inverter performance. A review of different active power decoupling techniques is presented in [36]–[38]. The aforementioned topologies are summarized in Table I regarding the number of switches and diodes.

This paper proposes a new single-stage ac module with series power decoupling capability for connecting PV to a single-phase power grid. It is able to handle the input and output power differences using small thin-film capacitors and a modified three-switch three-port flyback converter. It realizes power decoupling with just three switches and three diodes. To the best of our knowledge, it has the least number of switches among the inverters and microinverters proposed, previously.

This paper is organized as follows: The concept of power decoupling is discussed in Section II. The inverter circuit topology is introduced in Section III. Its operation principle and control strategy are presented in Sections IV and V, respectively. Section VI is dedicated to design considerations of the inverter. Experimental results are given in Section VII. Finally, the conclusion is presented in Section VIII.

II. Power Decoupling Concept

Fig. 1 shows a conventional grid-connected flyback inverter [39]. The input power is a constant value which is determined by the MPPT algorithm. The output power is time varying and includes both dc and ac parts. Assuming the inverter to be loss less and the grid voltage and the injected current as sinusoidal in-phase waveforms, dc part of the output power is equal to the input power and the ac part oscillates at double-line frequency. So, the instantaneous input and output powers can be written as follows:

$$P_{\rm PV} = V_{\rm PV} I_{\rm PV} \tag{1}$$

$$P_{\rm out}(t) = V_m I_m \sin^2 \omega t = P_{\rm PV}(1 - \cos 2\omega t). \tag{2}$$

In order to obtain a constant dc current at the input side, the oscillating part of the output power should be bypassed through

TABLE I
COMPARISON OF DIFFERENT POWER DECOUPLING METHODS

Reference	Switches	Diodes	Input Capacitance	Decoupling Capacitance	Efficiency	Control complexity
Kjaer and Blaabjerg [12]	6	4	–	314 μF	86.7%	Peak current control
Li *et al.* [**14**]	8	2	–	4 × 5.53 μF	–	Modified three-phase current modulation
Bush and Wang [15]	12	0	–	–	–	Three-phase voltage modulation
Shimizu *et al.* [17]	6	0	–	2 × 165 μF	70%	Three-phase voltage modulation
Tsuno *et al.* [18]	6	0	240 μF	2 × 150 μF	90.8%	Three-phase voltage modulation
Yao *et al.* [19]	4	0	–	2 × 60 μF	–	PR controller
Serban [21]	4	0	–	2 × 60 μF	90%	Control for bulk converters
Shimizu *et al.* [24]	4	3	20 μF	40 μF	70%	Peak current control
Tan *et al.* [26]	4	4	20 μF	50 μF	85%	Discontinuous-current control
Shinjo *et al.* [27]	9	7	44 μF	50 μF	–	Discontinuous-current control + power balance control
Cai *et al.* [28]	4	0	–	100 μF	93.5%	Power balance control
Hu *et al.* [30]	4	4	–	46 μF	89%	Peak current control + hybrid control
Hu *et al.* [31]	4	5	–	46 μF	89.8%	Peak current control + hybrid control
Ohnuma and Itoh [34]	5	1	–	30 μF	94.5%	Peak current control
Hirao *et al.* [33]	4	4	15 μF	44 μF	73%	Power balance control

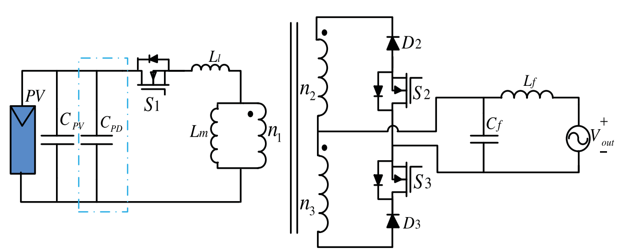

Fig. 1. Conventional grid-connected flyback inverter [34].

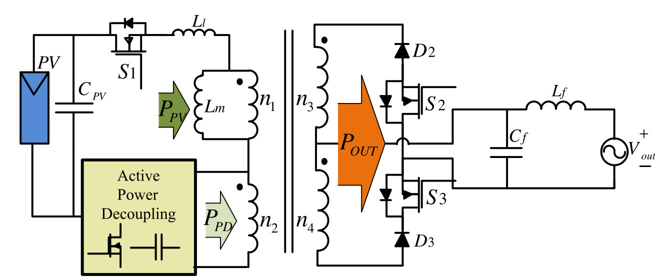

Fig. 2. Flyback inverter equipped with a power decoupling circuit.

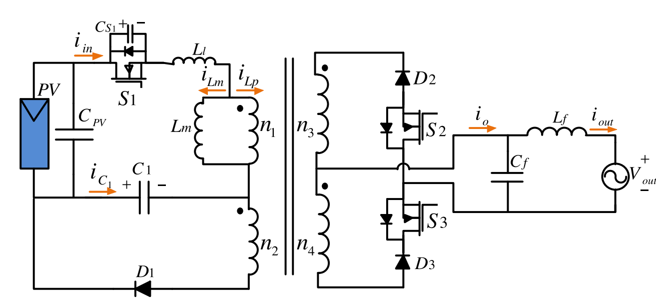

Fig. 3. Proposed inverter.

a buffer. The buffer instantaneous power should be equal to

$$P_{\rm PD}(t) = P_{\rm PV}\cos 2\omega t. \tag{3}$$

In a passive power decoupling circuit, a large electrolytic capacitor $C_{\rm PD}$ is placed across the PV to limit the voltage variation. However, electrolytic capacitors are sensitive to temperature and may decrease the inverter overall reliability.

Active power decoupling techniques are another method to compensate the power differences using long-lifetime thin-film capacitors and active switches. The switches are controlled in such a way that the extra energy is conveyed from PV to the decoupling capacitor when the input power is more than the output power. The energy of the decoupling capacitor transfers to the output when the input power is less than the required grid power. In three-port power decoupling methods, one port is dedicated for power decoupling, while the other two ports capture the input power and deliver it to the output. Fig. 2 demonstrates a three-port flyback inverter equipped with a power decoupling circuit.

Based on the power difference between the input and the instantaneous output powers, the operation of the inverter can be divided in two states. During *“state I,”* the input power is less than the output power and the decoupling capacitor is discharged. On the other hand, during *“state II,”* the input power is more than the output power and the decoupling capacitor absorbs energy and it is charged. Since the decoupling circuit just handles pulsating power, its average power is zero.

III. PROPOSED TOPOLOGY

The proposed ac module is shown in Fig. 3. It is a modified single-phase flyback inverter that is derived from the conventional flyback inverter by incorporating another transformer winding and an active power decoupling circuit. This three-switch inverter can extract maximum power from PV according to the MPPT algorithm, deliver a sinusoidal current to the grid, and compensate the input and output power differences using a small thin-film capacitor. These functions are easily realized by controlling switches $S_1 - S_3$.

The power decoupling circuit consists of diode D_1 and decoupling capacitor C_1. It does not utilize a separate switch for handling the pulsating power. However, the flyback main switch S_1 is exploited to store PV energy in the transformer as well

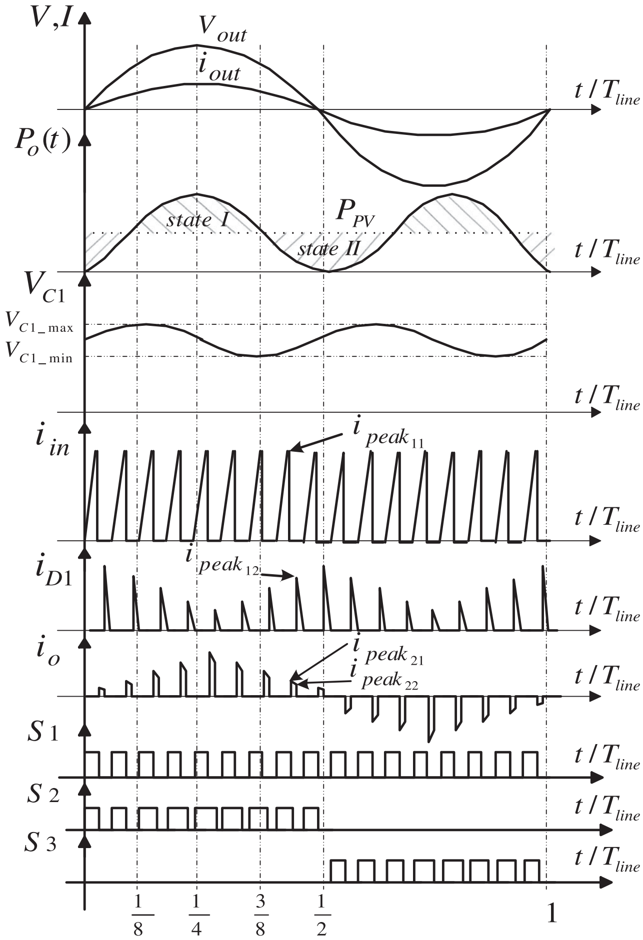

Fig. 4. Key waveforms of the proposed inverter.

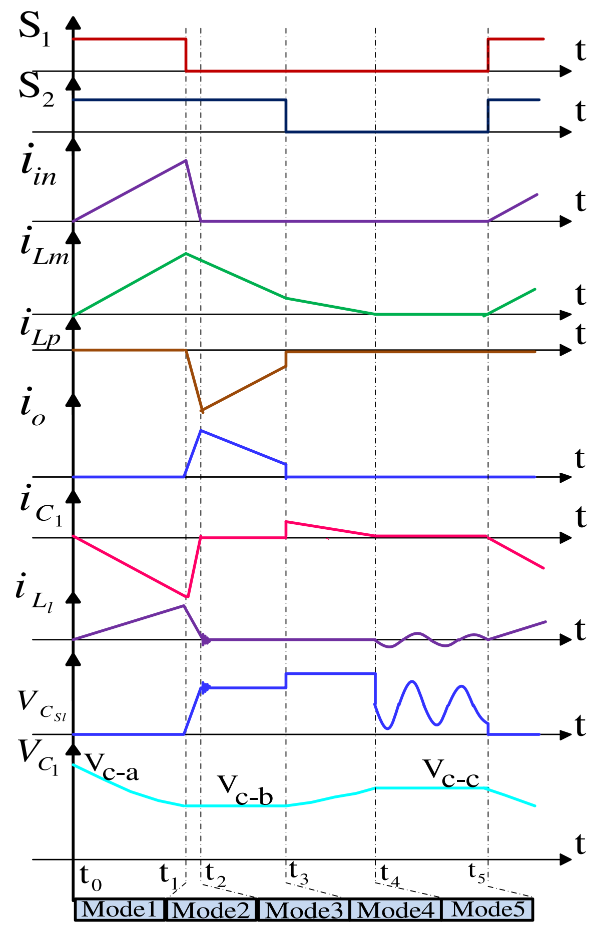

Fig. 5. Key waveforms during a switching period.

as buffering the pulsating energy. A snubber capacitor is placed across S_1 to reduce electromagnetic noise and provide soft-switching condition. The secondary-side diodes D_2 (D_3) and switches S_2 (S_3), connected in series, are responsible for transferring power from the PV side to the grid through appropriate transformer winding. The proposed inverter is connected to the grid through a low-pass filter to filter switching frequencies and delivers a low total harmonic distortion (THD) current to the grid.

The proposed inverter has some advantages including: 1) it has a simple structure, where only one diode and one capacitor are added to the transformer secondary winding to implement the power decoupling function; 2) it can implement MPPT, inject a sinusoidal current to the grid, and perform power decoupling using just three switches; and 3) the circuit operates in discontinuous-conduction mode (DCM) which benefits a simple control algorithm and soft-switching technique.

IV. Operation Modes and Analysis

Some key waveforms of the proposed inverter are depicted in Fig. 4. By turning switch S_1 ON, the energies of both PV and decoupling capacitor transfer to the transformer magnetizing inductance. When S_1 is turned OFF, while S_2 (S_3) is turned ON, a part of the flyback stored energy transfers to the grid through S_2 (S_3) and D_2 (D_3). By turning S_2 (S_3) off, the remaining energy of the transformer returns back to the decoupling capacitor through D_1. During *state I*, when decoupling capacitor feeds energy to the grid, the decoupling capacitor voltage decreases continuously until it reaches $V_{C1-\min}$ at the end of this state. In a similar manner, the decoupling capacitor stores energy during *state II* and its voltage reaches the peak value of $V_{C1-\max}$ at the end of *state II*.

The proposed inverter has five different operating modes during each switching period. The key waveforms of the inverter during a switching period and equivalent circuit of each operating mode are shown in Figs. 5 and 6, respectively. Since the inverter switching frequency is much higher than the power system frequency, the grid voltage and the reference current are almost constant during a switching period. It is assumed that the decoupling capacitor voltage V_{C1} is equal to V_{c-a} and all switches are off before the first subinterval. Moreover, it is assumed that the grid voltage is in the positive half cycle. The inverter operating modes are described as follows:

Mode 1 $(t_0 < t < t_1)$*:* Before this mode, the snubber capacitor C_{S1} and the transformer magnetizing inductance L_m are at resonance. At t_0, when the voltage across switch S_1 reaches its minimum value during the resonance, switches S_1 and S_2

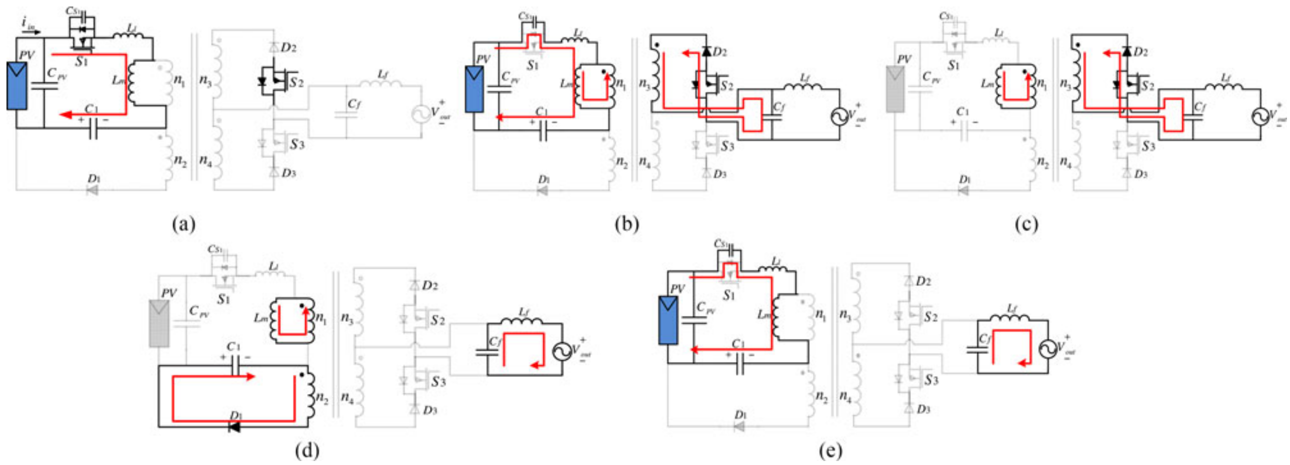

Fig. 6. Equivalent circuits during various operation modes. (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, and (e) mode 5.

are turned ON and S_3 is turned OFF. Therefore, switch S_1 is turned ON near zero voltage switching (ZVS) condition. Although S_2 is turned ON, it does not conduct any currents since the series-connected diode D_2 is reversed biased. Thus, S_2 is turned ON under zero current switching condition. The sum of PV and decoupling capacitor voltages is applied across the transformer leakage and magnetizing inductances during this operation mode. Since the circuit operates under the DCM condition, the transformer current increases linearly from zero and it can be expressed as

$$i_{\mathrm{Lm}}(t) = \frac{V_{\mathrm{PV}} + V_{C_1}}{L_m + L_l}(t - t_0). \tag{4}$$

This mode lasts until S_1 is turned OFF at t_1. At this time, the transformer's magnetizing inductance current reaches to the maximum value of i_{peak11}

$$i_{\mathrm{peak}_{11}} = \frac{V_{\mathrm{PV}} + V_{C_1}}{(L_m + L_l)f} d_1. \tag{5}$$

The input power can be calculated by averaging the input current as

$$P_{\mathrm{PV}} = \frac{1}{2} i_{\mathrm{peak}_{11}} d_1 V_{\mathrm{PV}}. \tag{6}$$

So, d_1 is determined by the following equation:

$$d_1 = \sqrt{\frac{2P_{\mathrm{PV}}(L_m + L_l)f}{V_{\mathrm{PV}}(V_{\mathrm{PV}} + V_{C_1})}}. \tag{7}$$

During this mode, some part of the decoupling capacitor energy is delivered to the transformer magnetizing inductance. Thus, its voltage decreases from V_{c-a} to V_{c-b} at the end of this mode. The increased amount of the magnetizing inductance energy during this mode is the sum of PV and decoupling capacitor energies. Consequently, the decoupling capacitor voltage at the end of this mode can be expressed as follows [40]:

$$V_{c-b} = \sqrt{V_{c-a}^2 + \frac{2d_1 V_{\mathrm{PV}} I_{\mathrm{PV}}}{C_1 f} - \frac{L_m}{C_1} I_{\mathrm{peak11}}^2}. \tag{8}$$

The equivalent circuit of this operating mode is shown in Fig. 6(a).

Mode 2 ($t_1 < t < t_2$): This mode, as shown in Fig. 6(b), is begun when S_1 is turned OFF at t_1. Since the capacitor C_{S1} is placed across S_1, the voltage of this switch increases smoothly and it is turned off under ZVS condition. This voltage starts from zero and finally reaches the value of V_{SS}

$$V_{\mathrm{SS}} = V_{C1} + V_{\mathrm{PV}} + n_{13} V_{\mathrm{out}}. \tag{9}$$

The current of the transformer leakage inductance gradually decreases until it reaches zero at the end of this mode. Since the duration of this mode is short and the magnetizing inductance is much larger than the leakage inductance, the magnetizing inductance current during this mode can be considered constant. The current of the transformer leakage inductance and the voltage of switch S_1 can be, respectively, expressed as

$$\begin{aligned} i_{L_l}(t) &= i_{\mathrm{peak}_{11}} \cos(\omega_0(t - t_1)) \\ &\quad + (V_{\mathrm{SS}}/Z_1)\sin(\omega_0(t - t_1)) \end{aligned} \tag{10}$$

$$\begin{aligned} V_{C_{S1}} &= V_{\mathrm{SS}}[1 - \cos(\omega_0(t - t_1))] \\ &\quad + (i_{\mathrm{peak}_{11}} Z_1)\sin(\omega_0(t - t_1)) \end{aligned} \tag{11}$$

where $Z_1 = \sqrt{L_l/C_{S_1}}$ and $\omega_0 = 1/\sqrt{L_l C_{S_1}}$. Since this mode is very short, the snubber capacitor voltage and leakage inductance current in (10) and (11) can be simplified as

$$i_{L_l}(t) = i_{\mathrm{peak}_{11}} + (V_{\mathrm{SS}}/L_l)(t - t_1) \tag{12}$$

$$V_{C_{S1}} = (i_{\mathrm{peak}_{11}}/C_{S_1})(t - t_1). \tag{13}$$

The time duration of this subinterval can be expressed as

$$\Delta t_{12} = t_2 - t_1 = C_{S_1} V_{\mathrm{ss}}/i_{\mathrm{peak}_{11}}. \tag{14}$$

Mode 3 ($t_2 < t < t_3$): In this mode, S_2 remains ON and some part of the stored energy in the flyback transformer is transferred to the grid through S_2 and D_2. The transformer output current at the beginning of this mode has a peak value of

$$i_{\mathrm{peak}\ 21} = n_{13} \frac{V_{\mathrm{PV}} + V_{C_1}}{(L_m + L_l)f} d_1. \tag{15}$$

This current deceases linearly until switch S_2 is turned OFF at t_3. Just before this moment, the output current reaches

$$i_{\text{peak 22}} = i_{\text{peak 21}} - n_{13}^2 \frac{d\,'|V_m \sin \omega t|}{L_m\, f}. \quad (16)$$

To have a sinusoidal current waveform in phase with the grid voltage, d' should be controlled in such a way that average value of the flyback output current be proportional to the output voltage. The energy that is delivered to the grid during this operation mode is equal to energy variation of the magnetizing inductance. Consequently, the magnetizing inductance current at the end of this mode can be related to its value at the beginning of this mode by [31]

$$i^2_{\text{peak 22}} = i^2_{\text{peak 21}} - \frac{2n_{13}^2 V_m I_m\, \sin^2 \omega t}{f L_m}. \quad (17)$$

Voltage of the decoupling capacitor is not changed during this mode. As shown in Fig. 6(c), this mode is terminated by turning S_2 OFF at t_3.

Mode 4 ($t_3 < t < t_4$)*:* Equivalent circuit of this mode is shown in Fig. 6(d). At t_3, switch S_2 is turned OFF and the remaining energy of the flyback transformer charges the decoupling capacitor through the transformer secondary winding and diode D_1. The magnetizing inductance current at the beginning of this mode is equal to

$$i_{\text{peak 12}} = \frac{i_{\text{peak 22}}}{n_{13}}. \quad (18)$$

This current decreases linearly until it reaches zero. Duration of this mode is calculated as follows:

$$\Delta t_{34} = t_4 - t_3 = \frac{L_m L_{\text{peak12}}}{n_{12} V_{C_1}}. \quad (19)$$

Voltage of the decoupling capacitor increases to V_{c-c} at the end of this mode. So, we have

$$V_{c-c} = V_{c-b} + \frac{L_m L^2_{\text{peak 12}}}{2n_{12} C_1 V_{C_1}}. \quad (20)$$

Voltage of switch S_1 in this mode is equals to

$$V_{\text{dd}} = V_{\text{PV}} + (1 + n_{12}) V_{C_1}. \quad (21)$$

Mode 5 ($t_4 < t < t_5$)*:* When the transformer's energy discharges totally to the decoupling capacitor at t_4, the circuit enters mode 5. At this time, a resonance happens between the snubber capacitor and the transformer magnetizing and leakage inductances. The inductance current and the snubber voltage during the resonance can be written as

$$i_{L_l}(t) = -(n_{12} V_{C_1}/Z_1\,') \sin(\omega_0'(t - t_4)) \quad (22)$$

$$V_{C_{S1}} = V_{\text{pp}} + n_{12} V_{C_1} \cos(\omega_0{}'(t - t_4)) \quad (23)$$

where $Z_1{}' = \sqrt{(L_l + L_m)/C_{S_1}}$, $\omega_0' = 1/\sqrt{(L_l + L_m) C_{S_1}}$, and $V_{\text{pp}} = V_{\text{PV}} + V_{C_1}$.

At the end of the switching period when the voltage of S_1 reaches its minimum value during resonance, S_1 is turned ON and this operation mode is finished. The duration of this mode can be expressed as

$$\Delta t_{45} = t_5 - t_4 = \frac{\pi(2k+1)}{\omega_0'}, k \in \mathbb{W} \quad (24)$$

where k is selected as

$$\Delta t_{45} \geq (T - \Delta t_{01} - \Delta t_{12} - \Delta t_{23} - \Delta t_{34}). \quad (25)$$

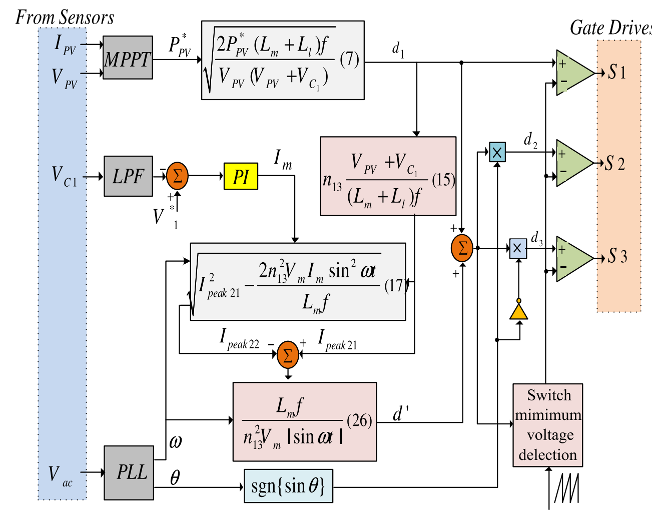

Fig. 7. Control block diagram of the proposed inverter.

V. Control Strategy

Block diagram of the proposed inverter is demonstrated in Fig. 7. It includes current and voltage sensors, phase-locked loop (PLL) block, MPPT controller, output current controller, half-cycle detection, etc. Voltages across the PV (V_{PV}), decoupling capacitor (V_{C1}), and grid (V_{ac}), as well as PV current (I_{PV}) are measured. The control strategy is designed to extract the maximum power from the PV and inject it to the grid with high quality.

An MPPT controller is utilized to extract maximum power from the PV panel according to the incremental conductance method [41]. The inverter is designed to operate under the DCM condition. By turning S_1 ON, energy is stored in the flyback transformer through both the PV and the decoupling capacitor. Duty cycle of switches S_1 should be determined according to the MPPT algorithm to satisfy (7).

Since the output current should be in phase with the grid voltage, a PLL block is employed to determine the voltage phase angle. This block is also used to recognize voltage positive and negative half cycles. The inverter will control S_2 and quench S_3 when the grid voltage is in the positive half cycle. It will turn S_2 OFF and control S_3 if the voltage is in the negative half cycle. Duty cycle of S_2 (S_3) is equal to d_1 plus d' which is derived from (15)

$$d\,' = \frac{L_m\, f}{n_{13}^2 V_m |\sin \omega t|}(i_{\text{peak 21}} - i_{\text{peak 22}}). \quad (26)$$

When MPPT controller increases the input power, average voltage of the decoupling capacitor is increased. Comparing this voltage to a reference value, amplitude of the output current I_m is increased too. More power is then delivered to the grid. As a result, I_m is varied such that the average voltage of the decoupling capacitor approaches the reference value. A low-pass filter is used to filter both the switching and 100-Hz ripple frequencies, which yields the average voltage of the decoupling capacitor.

VI. Design Considerations

The design process of the proposed inverter is presented in this section. The proposed inverter interfaces 60 V from the input PV panel to a 220-V 50-Hz power grid at the output. The decoupling capacitor's voltage is selected to have an average value of 100 V with a peak-to-peak ripple voltage of 40 V. So, the decoupling capacitor should be as low as 80 μF according to the following equation:

$$C_1 = \frac{2P_{\mathrm{PV}}}{\omega(V_{C_1-\max} - V_{C_1-\min})(V_{C_1-\max} + V_{C_1-\min})}. \quad (27)$$

Diode D_1 should be reverse biased during mode 3. Therefore, the transformer turn ratio n_{23} is determined to satisfy the following inequality under the worst-case condition:

$$n_{23} < \frac{V_{C_1}}{V_{\mathrm{out}}}. \quad (28)$$

The transformer turn ratio n_{12} determines S_1 and D_1 voltage stress. Higher values of n_{12} lead to high-voltage stresses on S_1 during operation in mode 4. On the other hand, lower values of this parameter cause higher voltage stresses on D_1 during operation mode 1. Choosing n_{12} to be unity, voltage stresses on S_1 and D_1 are become equal.

The proposed inverter should be able to inject power to the grid for the input voltage as low as 40 V. To have a 100-W input power, the input peak current i_{peak11} should be 16.66 A for the worst case of $V_{\mathrm{PV}} = 40$ V and $d_1 = 0.3$ according to (7). $L_m + L_l$ is then calculated using (5) to be 50.4 μH. Assuming the leakage inductance to be low enough, the magnetizing inductance is selected as 50 μH.

The maximum voltage on S_1 is occurred in mode 4 where the transformer primary winding reflects the decoupling capacitor's voltage and is equal to V_{dd}. Voltage stress on D_1 is given as follows:

$$V_{D_1} = V_{C_1} + \frac{V_{C_1} + V_{\mathrm{PV}}}{n_{12}}. \quad (29)$$

The voltage on $S_2\,(S_3)$ is maximum in mode 3 when the grid voltage is at its peak value and is equal to $2V_{\mathrm{m}}$. The peak voltage on $D_2\,(D_3)$ takes place when the grid voltage is at its peak value, and when $S_2\,(S_3)$ is turned on. In this case, the voltage stress is given as follows:

$$V_{D_2} = \frac{V_{C_1} + V_{\mathrm{PV}}}{n_{13}} + V_m. \quad (30)$$

VII. Experimental Results

To verify operation of the proposed inverter, a 100-W prototype inverter has been implemented, as shown in Fig. 8. A STM32F407VGT6 microcontroller with ARM Cortex-M4 32-bit MCU was adopted as the kernel in the implementation of the digital controller. A PV simulator is used as the input power source.

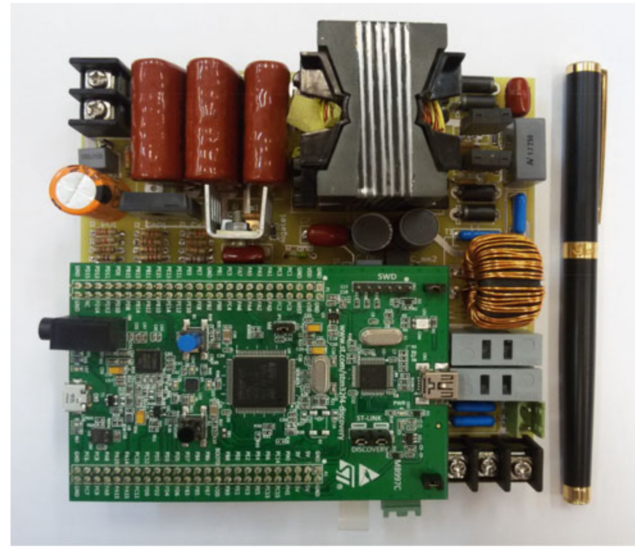

Fig. 8. Prototype of the proposed inverter.

TABLE II
KEY PARAMETERS OF THE PROTOTYPE INVERTER

Circuit parameters	**Value**
Input dc source voltage (V_{PV})	60 V
AC grid voltage (V_{rms})	220 V
Frequency of the ac grid voltage (f_{ac})	50 Hz
Nominal output power	100 W
Switching frequency (*f*)	50 kHz
Power decoupling capacitor (C_1)	80 μF
Filter capacitor (C_f)	15 μF
Capacitor across PV (C_{PV})	35 μF
Filter inductance (L_f)	1 mH
Transformer magnetizing inductance (L_m)	50 μH
Switch snubber capacitor (C_{S1})	4.7 nF
Transformer turn-ratios ($n_1 : n_2 : n_3 : n_4$)	1:1:4:4

TABLE III
DIODES AND SWITCHES MAIN SPECIFICATIONS

Switches/ Diodes	Part number	Specifications
S_1	IRFP4229PbF	$V_{\mathrm{DS}} = 300$ V, $R_{\mathrm{DS}} = 38$ mΩ
S_2 and S_3	STU7NB100	$V_{\mathrm{DS}} = 1000$ V, $R_{\mathrm{DS}} = 1.2\,\Omega$
D_1	STTH1602C	$t_{\mathrm{rr}} = 21$ ns, $I_f = 2 \times 10$ A, $V_D = 200$ V
D_2 and D_3	UF4008	$t_{\mathrm{rr}} = 75$ ns, $I_f = 1$ A, $V_D = 1000$ V

The key circuit parameters and their values are listed in Table II and the diodes and switches are specified in Table III.

The simulation results as shown in Fig. 9 depict some different voltage and current waveforms based on the actual parameter values. By turning S_1 OFF, its voltage gradually increases due to the snubber capacitor. So, S_1 is tuned OFF under ZVS condition.

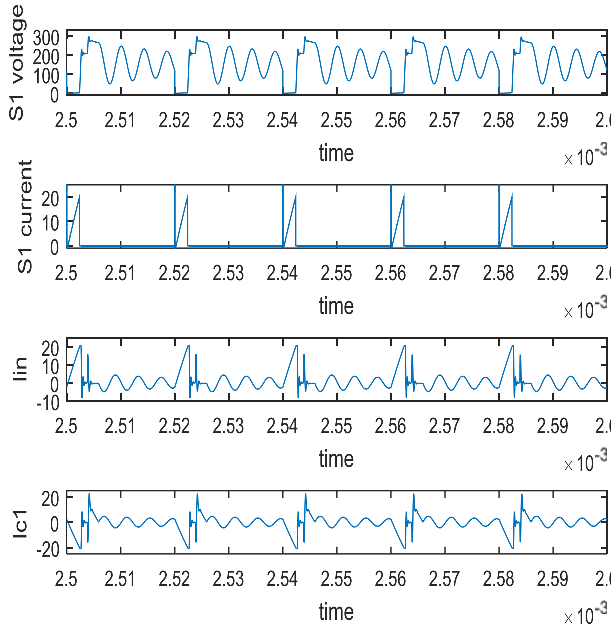

Fig. 9. Simulation results; voltage across switch S_1, current of switch S_1, inverter input current, and current of a decoupling capacitor.

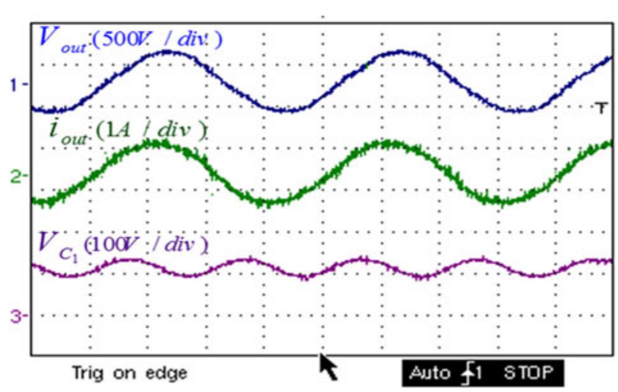

Fig. 10. Grid voltage, output current, and decoupling capacitor voltage, respectively (up to down).

Fig. 10 shows the experimental results of the grid voltage as well as output current and decoupling capacitor's voltage waveform. A power analyzer (C. A. 8335) measured the THD of the output current to be 3.5%. The output current is a sinusoidal waveform in phase with the grid voltage. It is obvious that the decoupling capacitor voltage has a pulsating part at the double-line frequency with 37-V peak to peak which is superimposed on an 110-V offset value. It is corresponding to (27) for delivering 100-W power to the grid.

The inverter output current before filtering and gate drive signals of switches S_1 and S_2 for positive half-line cycle are demonstrated in Fig. 11. S_3 is turned OFF and S_2 is switched such that a sinusoidal current after filtering is formed in the output. Duty cycle of S_2 is the same as S_1 when the grid voltage crosses zero. The S_2 duty cycle has the maximum value when the output voltage is at its peak.

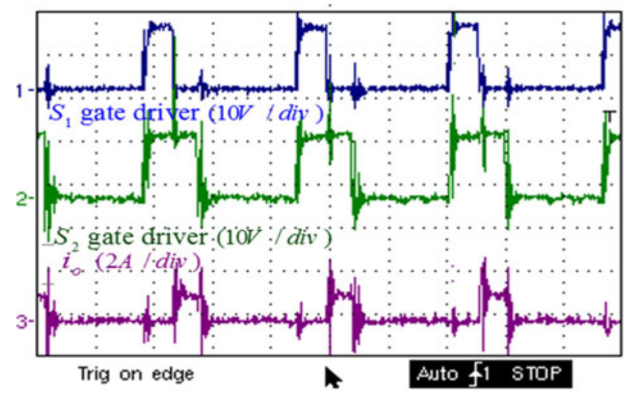

Fig. 11. Gate voltages of switches S_1, S_2, and the output current, respectively (up to down).

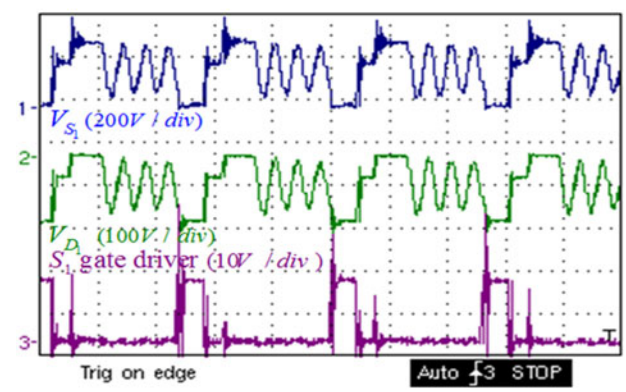

Fig. 12. Voltages of switch S_1 and diode D_1 and gate dive of switch S_2, respectively (up to down).

The gate-source and drain-source voltages of switch S_1 and diode D_1 voltages are depicted in Fig. 12. When S_1 is turned ON, D_1 voltage reaches the peak value of $-V_{C1} - (V_{C1} + V_{\mathrm{PV}})/n_{12}$. By turning S_1 off, while S_2 is turned ON, S_1 voltage is clamped to V_{SS} and D_1 voltage becomes $-V_{C1} + n_{23}V_{\mathrm{out}}$. When S_2 is turned OFF in mode 4, the voltage of S_1 is clamped to V_{dd} and the voltage of D_1 becomes zero.

Dynamic response of the proposed inverter is shown in Fig. 13. When PV voltage steps down from 55 to 40 V, the output power decreases from 62 to 35 W and the decoupling capacitor's ripple voltage decreases from 25 to 15 V. The control algorithm compensates the voltage variation of the decoupling capacitor within four cycles by decreasing the output power.

Efficiency of the proposed inverter is plotted in Fig. 14 versus its output power. The efficiency is calculated by dividing P_{OUT} by P_{IN} where the input and output powers are measured by the product of corresponding voltages and currents. The implemented inverter realizes maximum efficiency value of 91.1% for nearly half of the rated power, while its efficiency reaches 88.9% at the rated power.

Fig. 15 shows loss portions of different main components at the nominal output power. The loss of three switches and diodes as well as flyback transformer and filter inductance includes 94% of the total losses. Core loss is the main source of the inverter

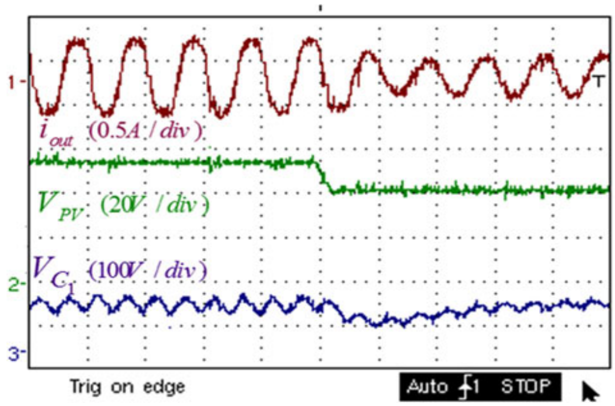

Fig. 13. Dynamic response of the proposed inverter.

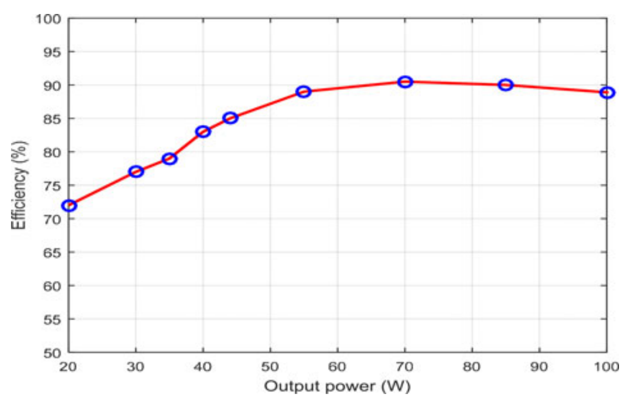

Fig. 14. Efficiency of the proposed inverter versus its output power.

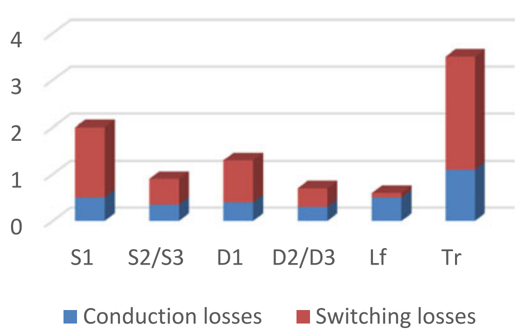

Fig. 15. Loss distribution of the main components.

losses. Implementing a larger core size and larger wire width can reduce core loss and improve the overall efficiency. Moreover, high-permeability (flux density) materials like amorphous or nanocrystalline cores can significantly enhance the efficiency of the microinverter but they will increase manufacturing cost.

VIII. Conclusion

A novel power decoupling method based on a three-switch three-port ac module has been proposed in this paper. The proposed circuit extracts maximum power from PV, handles ripple power, and delivers a low THD sinusoidal current to the grid with just three switches. Reliability of the microinverter is expected to be improved by decreasing the number of active switches. This economic, compact, and reliable inverter with a simple control strategy is an excellent candidate for PV low-power decentralized applications.

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